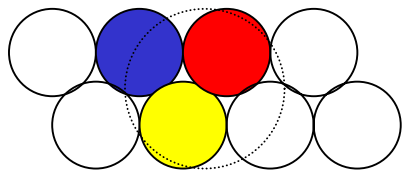
CTT Installation Plan

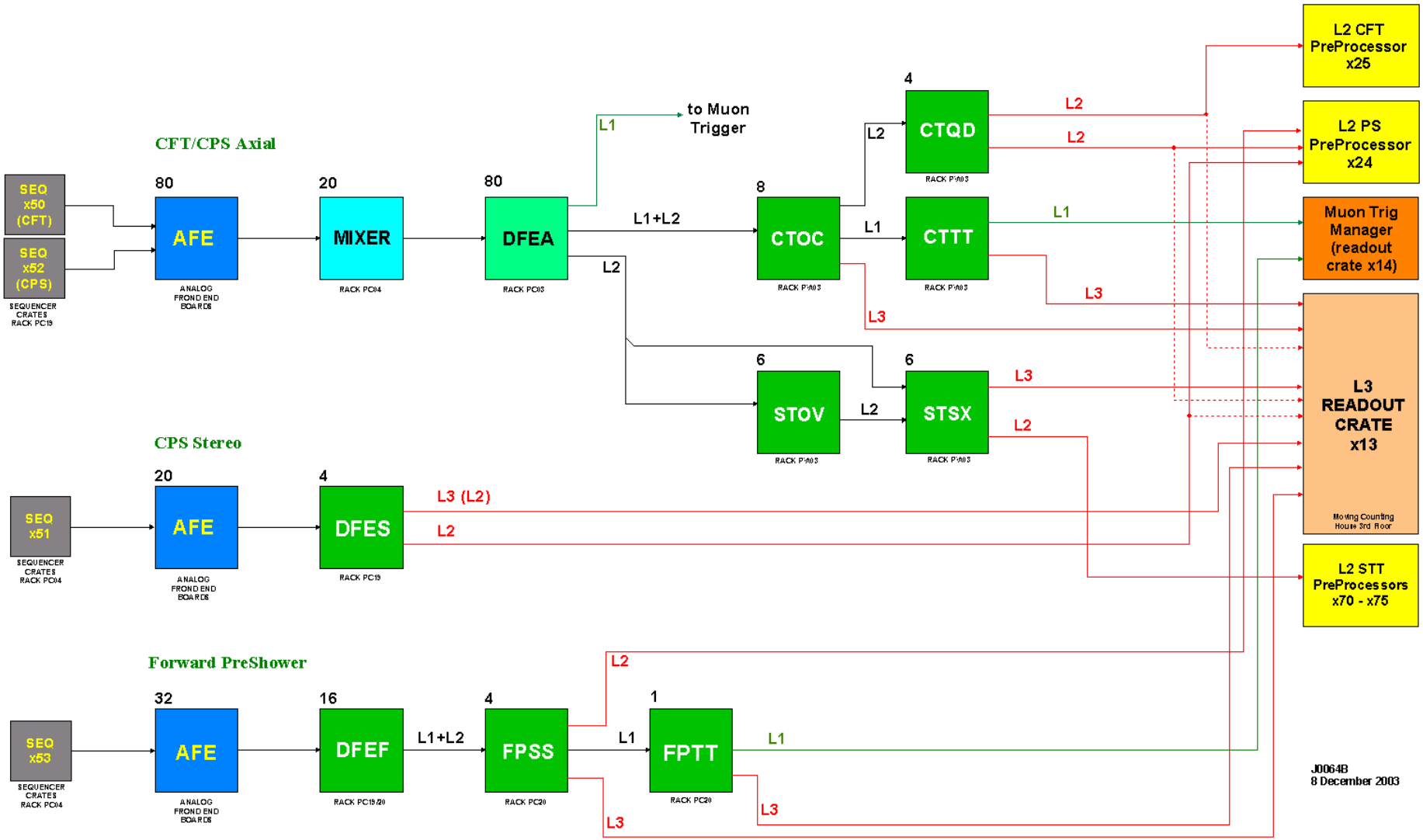
Current status
General plan
Power supplies + permits
Basic installation + checking procedures

Why upgrade?

- The existing CTT track finder (DFEA) performance is limited by logic resources in the Field Programmable Gate Arrays (FPGAs)
  - Xilinx Virtex FPGAs circa 1999, 600k gates
  - Track equations use 'doublet' groups of fibers
- More logic resources are now available
  - Virtex-II FPGAs are 10x larger, faster, lower power
  - Higher resolution track equations use 'singlet' fibers
  - Improved efficiency at higher luminosity
  - Better fake track rejection
- DFEA2 board design done at Boston University

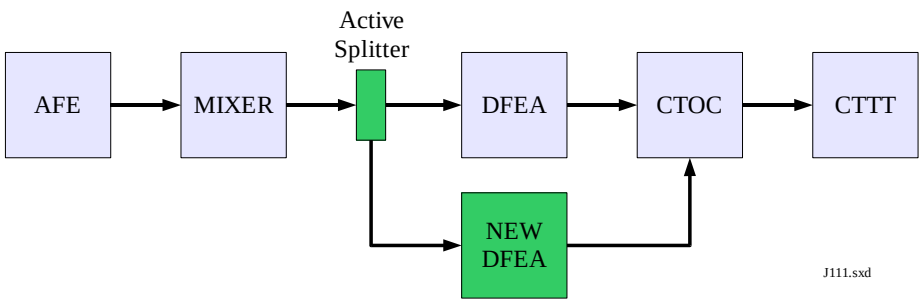


CTT System Overview

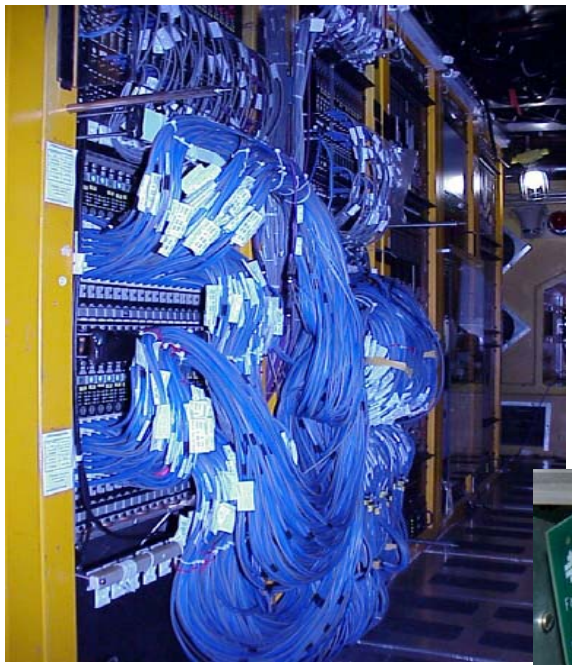


Status at FNAL

- Crates and boards in hand; new l1CalTrack cables terminated and DC-checked
- Power supplies and permit for parallel chain in place; need inspection after full crate installation to get permit for full system
- Installation location surveyed, basic procedure agreed upon
- 8 weeks for system and connections testing and repair (+ 8 weeks for physics commissioning)
- Doublet firmware shown to identically reproduce old system
- Singlet firmware: running in DFEA2s; no eff.known yet
- Control and monitoring software in place; first version exercised with parallel chain; full EPICS version under test now

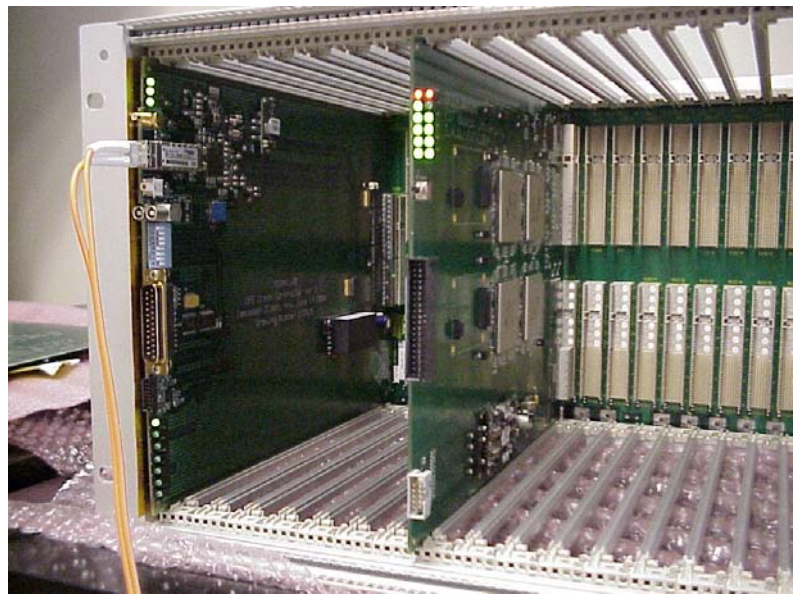


New Subrack and Backplane



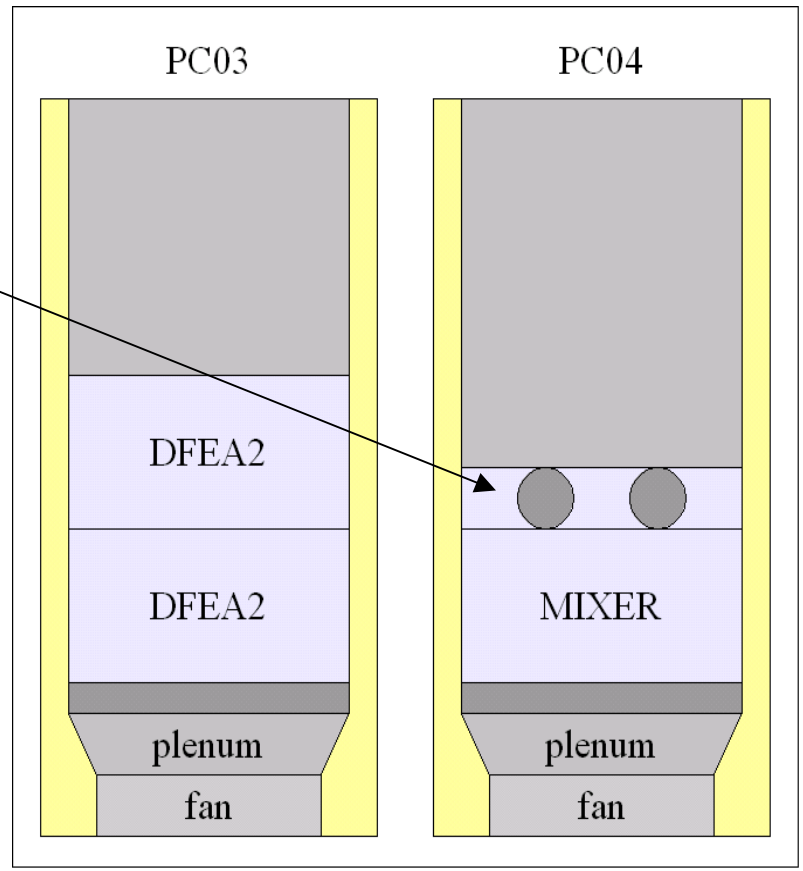
Improvements

- No more transition boards
- All cables pass through the backplane



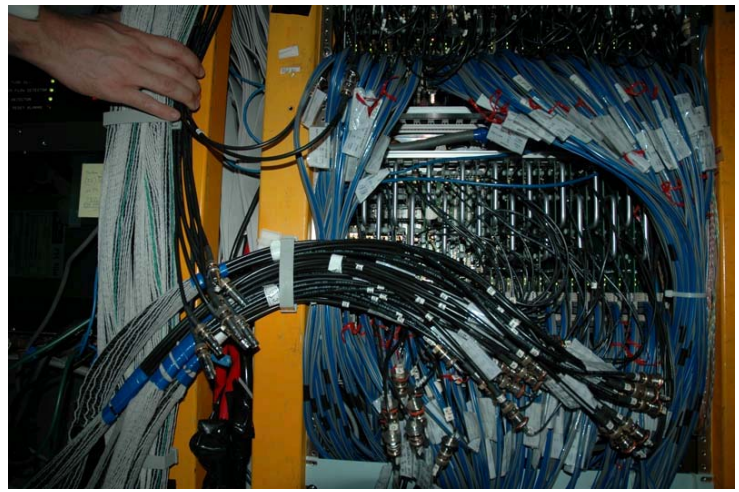
LVDS Cable Rerouting

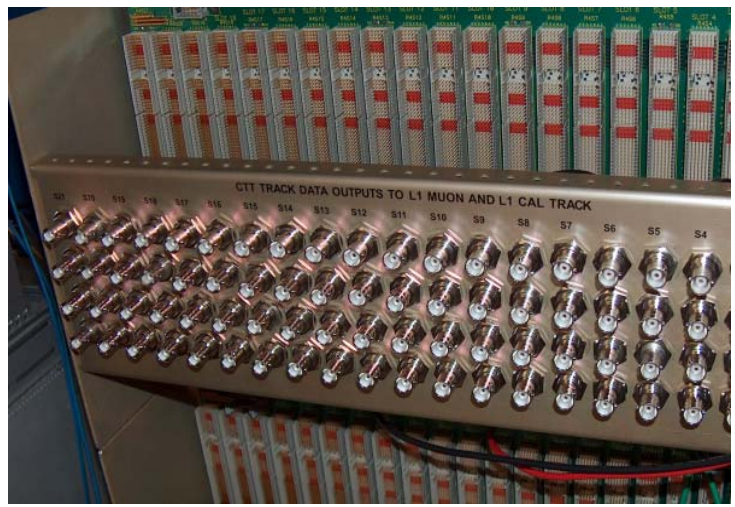
- Low voltage differential signal cables
  - 5 differential pairs
  - 1.7 Gigabits per second
- Cable tunnels will be installed in PC04 to allow the cables to reach the rear of PC03 and the DFEA2 crates
- Spare cables will be on hand (10%)



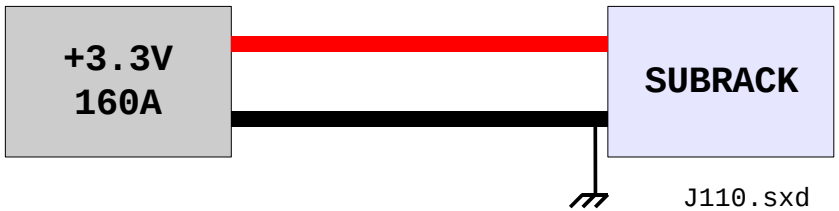
Muon and CalTrk Cables

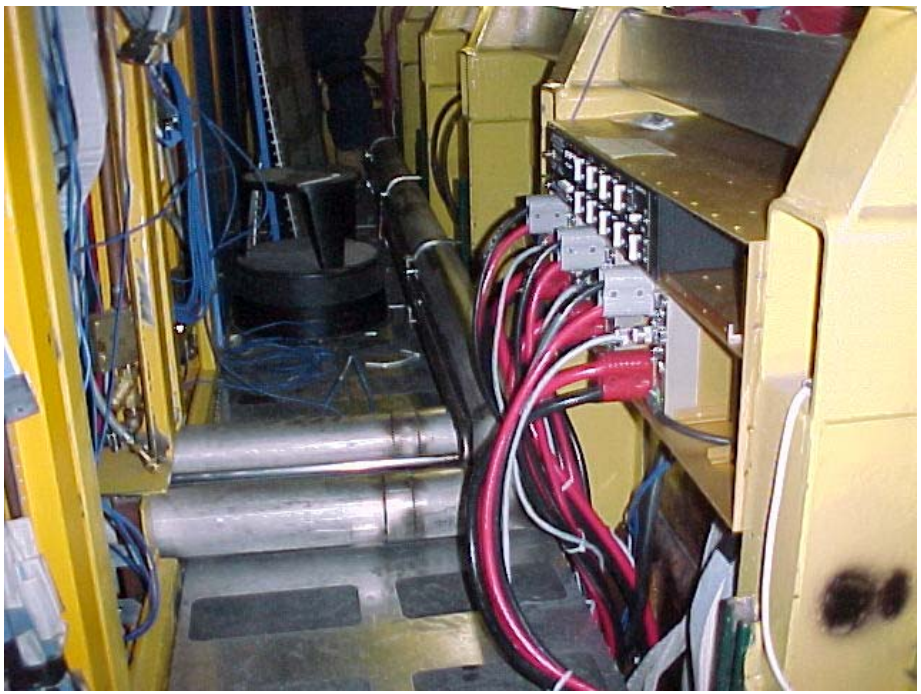
- 80 existing coaxial cables go to L1muon
- Adding 80 cables for L1caltrk
- New support bracket has been engineered to support the additional weight





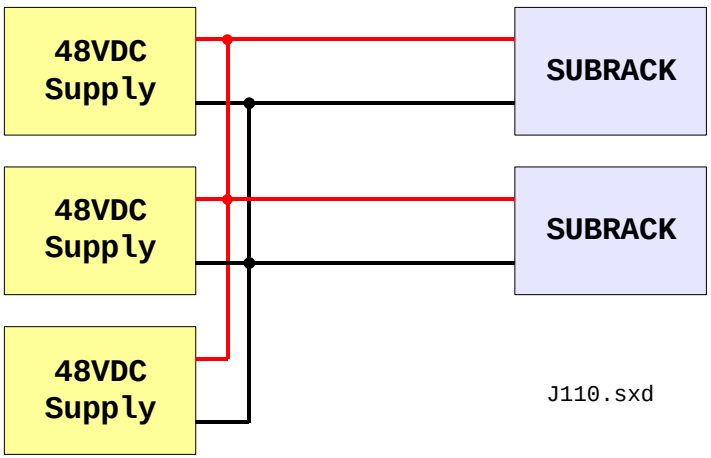
Low Voltage Power Supplies





- Our low voltage, high current supplies had problems with remote sense operation
- No redundancy: failure of a single supply means we lose a subrack
- Significant voltage drop even on thick cables
- Supplies must be located near the subrack
- Poor location with marginal cooling
- Half of the backplane was used for bus bars

Distributed Power Architecture



- 48VDC bulk supplies
- Parallel operation, N+1 redundancy
- Hot swap
- Excellent low voltage regulation on the boards using DC-DC converters
- Low EMI
- 36-72V input range
- Forget about remote sensing!
- No thick “welding cables”
- No bus bars on the backplane
- Logic voltages keep dropping: 1.5V, 1.2V, 1.0V…

CTT installation & commissioning

From the InstPhysCom plan:

- ***Software:***
- DFE Power Supply Control Update
- Ethernet Serializer
- DFEB (+CTOC) to dfe_ware DB
- Download Interface for DFEB to dfe_ware DB
- Link Test Scripts for Mixer-DFEB-CTOC Test
- DFEB firmware for Mixer-DFEB-CTOC Test
- DFEB+CTOC to Examine
- DFEB+CTOC to Offline Verification Codes
- trigsim equations for new (= singlet) and old equations

Preparing for Installation

- ***Hardware Precommission:***
- Establish SCL and GbE communication to CC
- Establish Crate Controller (CC) Operation
- Establish DFEB operation
- Load doublet equations into DFEB
- Load CTOC
- Load CTTT
- Load CTM with new CTTT map
- Link Tests for all new connections
- Observe 47712 Hz BOT
- Verify all I/O term rates
- Verify 0x13 output (old eqns)
- Verify 0x13 output (new eqns)
- Adjust firmware for rates, efficiency as modules added

- ***Hardware Commission:***
- Install boards
- Debug Inputs
- Verify Outputs
- Detailed study of Triggers

Installation Details

Hardware Install & Commission: 8 + 8 weeks (no beam + some beam)

- Check L1CalTrack cables using old DFEA system
- Install boards:
  - remove DFEA crates; replace baffle above Mixer with version with cable tunnels; retract Mixer-DFEA cables
  - Install DFEA2 crates; connect 48V; connect L1Muon and L1CalTrack cables to pigtails; connect Mixer-DFEA2 cables at backplane
- Debug Inputs: check clock/sync/parity status of DFEA2 using DFEA2 status reporting
- Verify Outputs:
  - check clock/sync/parity of CTOC/STSX/STOV/L1Muon/L1CalTrack inputs
  - Check trigger functionality using test vectors and DAQmon + CTT_examine
- Detailed study of Triggers: needs beam
  - L1: verify doublet firmware CTT And/Or rates are the same as before shutdown, using AOTmon; verify L1Muon outputs using L1Muon tools (e.g. TTK(1,10) version constructed by L1muon); ditto for L1CalTrack (using L1muon tools)
  - L2: Verify L2 outputs using STT examine and L2CTT/L2PS 'GM trigger examine'
  - L3: verify track triggers using GM examine; RECO outputs

CTT Shutdown Tasks w/o Beam

Personnel:

CTT physicists: Norik Khalatyan, Monica Pangilinan, Marc Buehler, Stefan Grünendahl

CTT engineer: Jamieson Olsen

Mixer engineer: Stefano Rapisarda

L1Muon-L1Caltrack group: Ken Johns, Susan Burke, Jeff Temple et al.

Technician for rack prep/metal work (Victor?)

STT expert

L2 expert

TASK	WHO	DURATION
Check L1CalTrack cables using old DFEA system	CTT phys, KJ et al.	1 day
remove DFEA crates	JO, 2*CTT phys	1/2 day
retract Mixer-DFEA cables	2*CTT phys	1/2 day
replace baffle above Mixer with version with cable tunnels	Tech, JO, CTT phys	2 days
Install DFEA2 crates	JO, 2*CTT phys	1 day
connect 48V	JO, CTT phys	1 day
connect L1Muon and L1CalTrack cables to pigtails	2*CTT phys	1 day
connect Mixer-DFEA2 cables at backplane	2*CTT phys, JO,SR	2-5 days
Debug Inputs: check clock/sync/parity status of DFEA2 using DFEA2 status reporting	3*CTT phys, JO	2-20 days
check clock/sync/parity of CTOC/STSX/STOV/L1Muon/L1CalTrack inputs	3*CTT phys, JO	2-20 days
Check trigger functionality using test vectors and DAQmon + CTT_examine	2*CTT phys	2-5 days

Backup Slides

CTT Commissioning (requiring Beam)

TASK	WHO	DURATION
L1: verify doublet firmware CTT And/Or rates are the same as before shutdown, using AOTmon	CTT phys	1-5 days
L1: verify L1Muon outputs using L1Muon tools (e.g. TTK(1,10) version constructed by L1muon)	CTT phys, KJ et al.	1-5 days
L1: verify L1CalTrack outputs using L1Muon tools	CTT phys, KJ et al.	1-5 days
L2: Verify L2 outputs using STT examine and L2CTT/L2PS 'GM trigger examine'	CTT phys, STT expert, L2 expert	1-3 days
L3: verify track triggers using GM examine; RECO outputs	CTT phys; D0 physics groups (trigger reps)	4 weeks